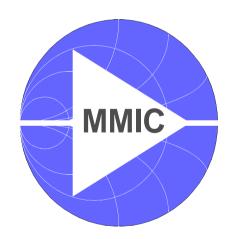
# BGA622L7

# Silicon Germanium Wide Band Low Noise Amplifier



Silicon Discretes



#### Edition 2004-11-04

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BGA622L7 Data Sheet Revision History:		2004-11-04	
Previous Version:		2004-07-27	
Page	Subjects (major changes since last revision)		

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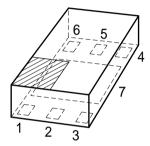


# Silicon Germanium Wide Band Low Noise Amplifier

#### **BGA622L7**

#### **Features**

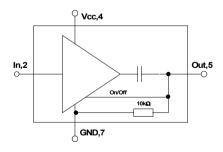
- High gain,  $|S_{21}|^2$ =17.5 dB at 1.575 GHz  $|S_{21}|^2$ =16.8 dB at 1.9 GHz  $|S_{21}|^2$ =16.2 dB at 2.14 GHz  $|S_{21}|^2$ =15.5 dB at 2.4 GHz
- Low noise figure, NF=1.0 dB at 1.575 GHz
- · Operating frequency range 0.5 6 GHz
- Typical supply voltage: 2.75V
- On/Off Switch
- Output-match on chip, input pre-matched
- Low external part count
- Tiny P-TSLP-7-1 leadless package
- 70 GHz f<sub>T</sub> Silicon Germanium technology



P-TSLP-7-1

### **Applications**

· LNA for GSM, GPS, DCS, PCS, UMTS, Bluetooth, ISM and WLAN



#### Description

The BGA622L7 is a wide band low noise amplifier, based on Infineon Technologies' Silicon Germanium Technology B7HF. The out-pin is simultaneously used for RF out and On/Off switch. This functionality can be accessed using a RF-Choke at the Out pin, where a DC level of 0 V or an open switches the device on and a DC level of Vcc switches the device off. While the device is switched off, it provides an insertion loss of 23 dB together with a high IIP3 up to 24 dBm at GPS frequencies.

**ESD:** Electrostatic discharge sensitive device, observe handling precaution!

Туре	Package	Marking	Chip
BGA622L7	P-TSLP-7-1	BR	T1535



### **Maximum Ratings**

Parameter	Symbol	Value	Unit
Voltage at pin Vcc	V <sub>cc</sub>	3.5	V
Voltage at pin Out	V <sub>OUT</sub>	4	V
Current into pin In	I <sub>IN</sub>	0.1	mA
Current into pin Out	I <sub>OUT</sub>	1	mA
Current into pin Vcc	I <sub>Vcc</sub>	10	mA
RF input power	P <sub>IN</sub>	6	dBm
Total power dissipation, T <sub>S</sub> < 142 °C <sup>1)</sup>	P <sub>tot</sub>	35	mW
Junction temperature	Tj	150	°C
Ambient temperature range	T <sub>A</sub>	-65 <b>+</b> 150	°C
Storage temperature range	T <sub>STG</sub>	-65 <b>+</b> 150	°C
Thermal resistance: junction-soldering point	R <sub>th JS</sub>	240	K/W

 $<sup>^{1)}</sup>$   $T_{\rm S}$  is measured on the ground lead at the soldering point

Note: All Voltages refer to GND-Node

# Electrical Characteristics at $T_A$ =25°C (measured according to fig. 1) Vcc=2.75 V, Frequency=1.575 GHz, unless otherwise specified

Parameter	Symbol	min.	typ.	max.	Unit
Insertion power gain	$ S_{21} ^2$		17.5		dB
Insertion power gain (Off-State)	$ S_{21} ^2$		-23		dB
Input Return Loss (On-State)	RL <sub>IN</sub>		6		dB
Output Return Loss (On-State)	RL <sub>OUT</sub>		13		dB
Noise Figure ( $Z_S=50\Omega$ )	$F_{50\Omega}$		1.0		dB
	IIP <sub>3</sub>		-2		dBm
	IIP <sub>3</sub>		24		dBm
Input Power at 1dB Gain Compression	P <sub>-1dB</sub>		-20		dBm
Total Device Off Current, V <sub>CC</sub> =2.75V, V <sub>out</sub> =V <sub>CC</sub>	I <sub>tot-off</sub>		260		μA
Total Device On Current, V <sub>CC</sub> =2.75V	I <sub>tot-on</sub>		5.8		mA

 $<sup>^{1)}</sup>$  IP3 value depends on termination of all intermodulation frequency components. Termination used for this measurement is 50  $\Omega$  from 0.1 to 6 GHz

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# Electrical Characteristics at $T_A$ =25°C (measured according to fig. 1) Vcc=2.75 V, Frequency=2.14 GHz, unless otherwise specified

Parameter	Symbol	min.	typ.	max.	Unit
Insertion power gain	$ S_{21} ^2$		16.2		dB
Insertion power gain (Off-State)	$ S_{21} ^2$		-20		dB
Input Return Loss (On-State)	RL <sub>IN</sub>		7		dB
Output Return Loss (On-State)	RL <sub>OUT</sub>		13		dB
Noise Figure ( $Z_S=50\Omega$ )	$F_{50\Omega}$		1.1		dB
$\overline{\text{Input Third Order Intercept Point}^{1)}  (\text{On-State})} \\ \Delta \text{f=1MHz},  P_{\text{IN}} \text{=-28dBm}$	IIP <sub>3</sub>		0		dBm
	IIP <sub>3</sub>		22		dBm
Input Power at 1dB Gain Compression	P <sub>-1dB</sub>		-16		dBm

 $<sup>^{1)}</sup>$  IP3 value depends on termination of all intermodulation frequency components. Termination used for this measurement is 50  $\Omega$  from 0.1 to 6 GHz

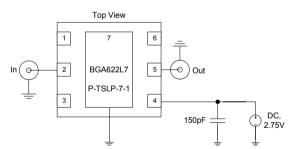
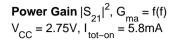
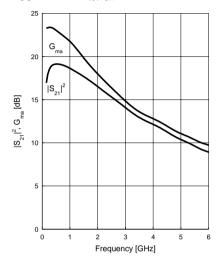


Figure 1 S-Parameter Test Circuit (loss-free microstrip line)

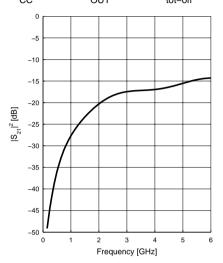
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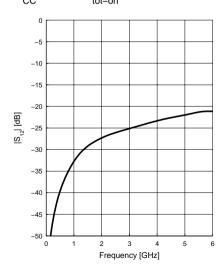




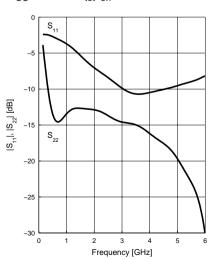
$$\begin{aligned} & \text{Off Gain } |S_{21}|^2 = \text{f(f)} \\ &V_{CC} = 2.75 \text{V}, \, V_{OUT} = 2.75 \text{V}, \, I_{tot-off} = 0.3 \text{mA} \end{aligned}$$



Reverse Isolation 
$$|S_{12}| = f(f)$$
  
 $V_{CC} = 2.75V$ ,  $I_{tot-on} = 5.8mA$ 

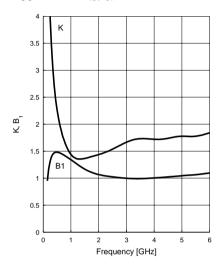


$$\begin{aligned} & \textbf{Matching} \ |S_{11}|, \ |S_{22}| = f(f) \\ &V_{CC} = 2.75V, \ I_{tot-on} = 5.8 mA \end{aligned}$$

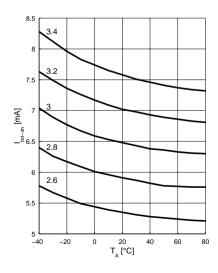




## Stability K, B<sub>1</sub> = f(f) $V_{CC} = 2.75V$ , $I_{tot-on} = 5.8mA$

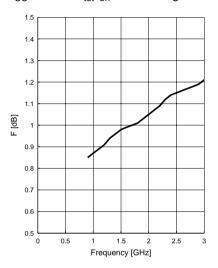


# **Device Current** $I_{tot-on} = f(T_A, V_{CC})$ $V_{CC} = parameter in V$

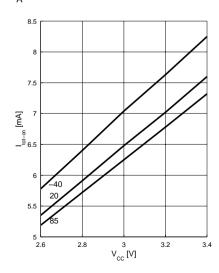


### Noise Figure F = f(f)

$$V_{CC} = 2.75V$$
,  $I_{tot-on} = 5.8$ mA,  $Z_{S} = 50\Omega$ 

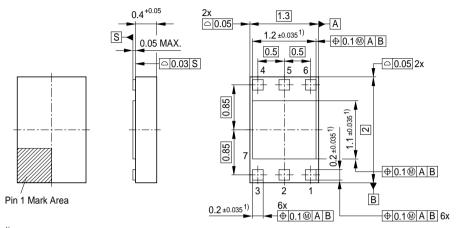


# $\begin{array}{l} \textbf{Device Current I}_{\text{tot-on}} = f(V_{\text{CC}}, \, T_{\text{A}}) \\ T_{\text{A}} = \text{parameter in } ^{\circ}\text{C} \end{array}$





### **Package Outline**



<sup>1)</sup> Dimension applies to plated terminals

### Tape loading orientation

